Amendments to the Claims

Prior to examination, please cancel claims 1 through 15.

Please add claims 16-25.

1-15. (canceled)

16. (original) A flash memory with a NOR-gate architecture, comprising:

a data block allocated to storage of erase and write times for other data blocks in the flash memory.

17. (original) A memory system, comprising:

a processor; and

a memory bank having data blocks, comprising:

a system table accessible by the processor to store data about the data blocks; and

at least one erase and write table accessible by the processor to store erase and write time data for the data blocks.

18. (original) The memory of claim 17 wherein the processor is in communication with a host computer.

19. (original) The memory of claim 18 wherein the host computer is a dedicated Internet device.

20. (original) The memory of claim 16 wherein the erase and write table also stores data about a total number of bytes for each storage operation.

21. (original) The memory of claim 16 wherein a table also stores number of erasures for each data block.

22. (original) The system of claim 16, wherein the system table is stored in a data block.

23. (original) The system of claim 16, wherein the erase and write table is stored in a data block.

24. (original) The system of claim 16, wherein the data blocks are organized into data banks and the system table and the erase and write table are in the same data bank.

25. (original) The system of claim 16, wherein the data blocks are organized into data banks and the system table and the erase and write table are in different data banks.